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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/705,134	11/02/2000	Alan E. Reamon	PD-99W231	6154

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EXAMINER	
LEE, BENNY T	
ART UNIT	**PAPER NUMBER**
2817	

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Please find below and/or attached an Office communication concerning this application or proceeding.

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FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.

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DATE MAILED:

...from the examiner in charge of your application.
...TENTS AND TRADEMARKS

☐ This application has been examined ☒ Responsive to communication filed on 9 Jan 2004 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire Three (3) month(s), _____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, Form PTO-152
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 1, 7, 12 are pending in the application.

   Of the above, claims _____ are withdrawn from consideration.

2. ☒ Claims 11 has been cancelled.
3. ☒ Claims 12 are allowed.
4. ☒ Claims 1, 7 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____, has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

PTOL-326 (Rev.9-89)

EXAMINER'S ACTION

SN 705134

U.S.GPO:1990-259-282

The disclosure is objected to because of the following informalities: In the description of Fig. 5, it is again requested that reference labels (16^{IV}, 16^{V}, 16^{VI}) be described in the specification. Applicants' comments regarding the inclusive series of superscripted labels have been noted. However, since these reference labels have been explicitly provided for in Fig. 5, they must be correspondingly described in the specification description thereof. Appropriate correction is required.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the connection of "circuit elements" by the "on-chip multi-layered metal-shielded monolithic transmission line" (e.g. amended cls 1, 12) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The specification needs to provide a description of the "plurality of circuit elements" being interconnected by the "on-chip multi-layer metal-shielded monolithic transmission line" as recited by amended claims 1, 12.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 7 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Gaibotti et al.

Gaibotti et al (figs 1 & 2) discloses a shielded transmission line structure used as an electrical connection between circuit components "inside an integrated circuit" (i.e. on-chip) as described at the Background of the Invention (i.e. col 1, ls 10-21). As evident from Fig. 1, the shielded transmission line comprises a plurality of thin film conductive layers arranged in a stacked arrangement (i.e. S2, S1-IS, S3) with an initial layer (S2) and a final layer (S3) providing bottom & top conductive planes, respectively. Although not explicitly shown in the drawings, non-conductive film layers inherently are disposed between alternate conductive thin film layers since integrated circuits are known to include layers of non-conductive material to support the conductive layers and circuit components therein. Note in particular that the intermediate conductive layer includes a signal conductor (S1) and intermediate conductive or terminal structures (IS) laterally spaced by a distance on both sides of signal conductor (S1). Moreover, as evident from Fig. 2, a plurality of contact structures (CN) comprised of spaced conductive openings or vias are disposed between and electrically connecting the intermediate conductive structures (IS) and bottom conductive plane (C2) as described at col 3, ls 3-5. In a similar manner, plural vias (VS) comprised filled metal openings electrically connecting the conductive plane (S3) to the intermediate conductive structures (IS) as described at col 2, ls 65-67.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ma in view of Gaibotti et al.

Ma (Fig. 2) discloses a shielded on-chip transmission line structure (100) formed as part of an integrated circuit device and providing interconnection between circuit elements on the integrated circuit (e.g. see Fig. 1). As evident from fig. 2, the shielded on-chip transmission line comprises respective lower and upper conductive thin film layers (104, 102) and an intermediate signal layer (90) arranged as a stacked arrangement. Furthermore, as evident from figs. 8-15, note that the shielded structure also includes intermediate non-conductive film layers (128, 130). However, as evident from figs. 1 & 13-15, that solid conductive walls (106, 108) electrically connect with upper and lower conductive layers (102, 104) as opposed to the claimed plurality of conductive vias interconnecting the upper and lower planes through intermediate terminal strips as recited in claim 1.

As described above, Gaibotti et al (figs. 1, 2) also discloses a shielded transmission line structure for an integrated circuit which includes upper and lower conductive layers (S3, S2) interconnected through a plurality of vias (VS), laterally spaced intermediate terminal conductive layers and conductively filled contacts structure (CN) to form the shielded sidewalls of the shielded transmission line. Furthermore, as evident from fig. 3, an alternative arrangement is to provide a solid vertical continuous conductive layer (CN) to form the shielded sidewalls of the shielded transmission line. However, as described at col 3, ls 7-19, the use of the continuous contact structure (i.e. Fig. 3) requires more space but provides better shielding while the

alternative yet equivalent via/contact structure (i.e. Figs. 1, 2) requires less space and provides adequate shielding.

Accordingly, it would have been obvious in view of the references, taken as a whole, to have modified the vertical shielding sidewalls (106, 108) of Ma to have been a via/contact structure with an intermediate terminal layer as taught by Gaibotti et al. Such a modification would have been considered an obvious substitution of art recognized equivalent shielded side wall structures, especially since Gaibotti et al explicitly recognizes the equivalent nature of each sidewall structure, thereby suggesting the obviousness of the combination. Furthermore, as recognized by Gaibotti et al, the use of the via/contact structure for a shielded sidewall would have provided the advantageous benefit of less space yet provide adequate shielding, thereby further suggesting the obviousness of such a combination.

Applicant's arguments with respect to claims 1, 7; 11 have been considered but are moot in view of the new ground(s) of rejection.

Claim 12 is allowable over the prior art of record.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Weiling pertains to a shielded interconnect structure of an integrated circuit..

Any inquiry concerning this communication should be directed to Benny Lee at telephone number 571 272 1764.

B. Lee

BENNY T. LEE
PRIMARY EXAMINER
ART UNIT 2817